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10EC751

Seventh Semester B.E. Degree Examination, June/July 2015
DSP Algorithm and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With neat block diagram, explain digital signal processing system. **(04 Marks)**

b. Explain common features of programmable digital signal processor. **(08 Marks)**

c. Explain decimation and interpolation process. **(08 Marks)**

2 a. Write the structure of 4 × 4 Braun multiplier and explain its concept. **(06 Marks)**

b. It is required to find sum of 256 numbers each is represented by 16 bits. How many bits should the accumulator have so that the sum is computed without overflow? It is decided to have a accumulator with 16 bits, by how many bits each number is shifted to avoid overflow? **(04 Marks)**

c. With the help of block diagram, explain program sequencer. **(06 Marks)**

d. Write the block diagram of parallel implementation of 8 – tap FIR filter using two MAC units. **(04 Marks)**

3 a. With neat diagram,, explain barrel shifter of TMS320C54XX processor. **(05 Marks)**

b. With the help of block diagram, explain direct addressing mode of TMS320C54XX processor. **(05 Marks)**

c. The register AR4 with contents 1010H is selected as pointer for circular buffer. If circular buffer size is 48, what would be loaded into circular buffer size (BK) register? Determine start address and end-address of buffer. What would be the contents of AR4 after execution of the instruction *AR4 + 0%, A, if contents of AR0 register is 0025H? **(05 Marks)**

d. Explain processor mode status (PMST) register of TMS320C54XX processor. **(05 Marks)**

4 a. Describe the operation of following instructions :

i) MAC *AR3 –, *AR4 +, B, A

ii) MPY *AR5 –, *AR4 + 0, B

iii) RPT #8. **(06 Marks)**

b. Show the pipeline operation of following sequence of instructions, if initial value of AR1, AR3, and A are 84, 81, 1 and value stored in memory locations 81, 82, 83, 84 are 2, 3, 4, 6. Also provide values of registers AR3, AR1, A after completion of each cycle.

ADD *AR3 +, A
LD *AR1+, T
MPY *AR3+, B
ADD B, A. **(08 Marks)**

c. With the help of logical block diagram, explain hardware timer circuit. **(06 Marks)**

PART – B

5 a. Represent both $N_1 = 0.5$ and $N_2 = 0.25$ in Q15 number notation and write assembly language program for TMS320C54XX processor to multiply obtained Q15 numbers. **(06 Marks)**

b. Determine the value of each of the following 16-bits numbers represented using Q-notation.
   i) 4400h as a Q7 number
   ii) 4400h as a Q0 number
   iii) 2ccch as a Q15 number
   iv) E6EFh as a Q15 number. **(04 Marks)**

c. Show the memory organization for digital interpolation using 15 tap FIR filter with interpolation factor 5. **(04 Marks)**

d. What is the drawback of linear interpolation filter? Explain the scheme to overcome this drawback. **(06 Marks)**

6 a. Why scaling is required before or during butterfly computation? Draw the butterfly computation that uses 0.25 as scale factor. **(04 Marks)**

b. Determine the following for a 128 point FFT computation :
   i) Number of stages
   ii) Number of butterflies in each stage. **(02 Marks)**

c. With an example, explain bit reversed index generation in TMS320C54XX DSP. **(08 Marks)**

d. Write the subroutine program to find the spectrum transformed data using TMS320C54XX DSP. **(06 Marks)**

7 a. With neat timing diagram, explain external memory interface singles of TMS320C54XX processor for read-read-write operations. **(10 Marks)**

b. Discuss the interrupt handling in TMS320C54XX processor. **(10 Marks)**

8 a. With the help of block diagram, explain synchronous serial interface between TMSC54XX and CODEC. **(04 Marks)**

b. Explain the building blocks of PCM3002 CODEC. **(08 Marks)**

c. With the help of block diagram, explain JPEG algorithm. **(08 Marks)**

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